Model DA924

High Resolution Digital to Analog Converter

Operations Manual

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Introduction

The DA924 converts incoming digital inputs to 24 bit analog audio signals. The combination of excellent linearity, small quantization steps, fast and accurate response and low noise performance enables reproduction of the finest details. The DA924 accommodates today's standard sample rates (40-50KHz) and the higher rates of the new standards (80-100KHz).

The DA924 provides many enhancements to the classical resistor weighting architecture. A **triple segmented design** improves the accuracy of the 10 most significant bits. Short-term accuracy is maintained by keeping the critical components at constant temperature in a **linearly controlled oven.** Long term accuracy is achieved by extensive use of continuous **automatic self-calibration**.

A large number of **extra codes** enable the addition of digital DC offset to the signal path without signal clipping. The DC offset provides superior low level detail by keeping low level signals away from the most significant bit transitions. A **quad switch deglitcher circuit** removes the unwanted transition glitch energy.

The DA924 **eliminates jitter** in the incoming data stream by use of a DSP controlled pullable crystal oscillator and a short buffer memory for temporary storage of the incoming data. The DSP transfers the data from the memory to the DAC disregarding any jitter in the input frequency. A proprietary fast-lock high-accuracy measurement compares the average input frequency to the oscillator frequency and makes the appropriate adjustments. The adjustments are done with sub pico-second resolution, to insure minimum interference with signal reconstruction.

Additional features:

- **96kHz, 88.2kHz, 48kHz and 44.1kHz conversion frequencies**
- **Multi-bit architecture with 24 bits, non Sigma-Delta**
- **Very low Total Harmonic Distortion + Noise**
- **Automatic calibration**
- **Increased low level accuracy**
- **CrystalLock™ Digital Jitter removal**
- **Professional and consumer inputs and outputs**
- **Supports New Hi-density I/O Standards from Sonic Solutions**

PART I: Operating Instructions

Operation of the **Model DA924 Digital to Analog Converter** requires the use of two push button switches located on the front panel.

POLARITY inverts the absolute polarity of the signal.

INPUT SELECT controls selection of digital inputs to the DAC.

Input signal selection

The **INPUT SELECT** lamp indicators show the selected input signal. Pressing the **INPUT SELECT** push button moves to the next input position.

Holding the **INPUT SELECT** button for more then a second makes the **DA924** go into search mode: the unit will step through the inputs but will skip the inactive input connectors (where no signal is present).

Holding the **INPUT SELECT** button for more than one second switches between manual input selection and the input search mode, or visa versa. The mode selected is retained when power is removed.

Input signal connection

The unit can be connected to one, two or three digital input connectors located on the rear panel:

AES/EBU input to the XLR connector designated as **AES INPUT 1**
AES/EBU input to the XLR connector designated as **AES INPUT 2**
SPDIF (consumer format) input to **IEC INPUT**.

Analog Outputs

The **LEFT OUTPUT** and **RIGHT OUTPUT** XLR signals are factory set to provide Balanced analog signals (signal between pin 2 and pin 3 of the XLR connectors).
Operation in unbalanced mode (signal at pin 2 and ground at pin 3) is possible by changing the internal jumpers J8 and J10 located behind the XLR analog output connectors inside the case.

The factory default setting is for Balanced outputs-- the jumpers are positioned parallel to the front panel.

For Unbalanced mode position, the jumpers are set to 90 degrees with respect to the front panel.

Pin 1 of the XLR connectors is connected to ground potential for proper cable shield connection.

The LEFT **OUTPUT** and **RIGHT OUTPUT** IEC signals are always unbalanced and are not effected by J8 and J10 jumper settings.

Analog Output Level Adjustment

Level control trim pots are located between the **LEFT OUTPUT** and **RIGHT OUTPUT** XLR connectors. When hooked for balanced output, the full-scale analog level can be adjusted between 12dBu to 22dBu.

When hooked for Unbalanced output, the full-scale analog level can be adjusted between 6dBu to 16dBu.

The IEC connector level is adjustable between 8dBu and -8dBu full-scale signal.

The wide 0-10dB attenuation range relies on an internal pot. When operating at minimum attenuation (22dBu balanced or 16dBu unbalanced), the signal is tapped directly from the top of the pot, thus the pot is effectively out of the signal path. Increasing the attenuation introduces more and more pot resistance into the signal path.

While taking all precautions to minimize sonic degradation associated with use of pots in the signal path, we offer alternative factory settings, trading off the adjustment range from 21dB to 2.8dB (+/-1.46dB). These settings minimize the impact of the pot on sonic quality, and may be of interest for users willing to have the unit set for operation with a very low range of level adjustment. Contact the factory for more information.

Turn-On sequence

When applying AC power to the unit, the following sequence of events take place:

1. The unit goes into mute mode.

2. Warm-up: An internal oven heats up the temperature-sensitive devices to a set temperature. The warm-up time depends on the initial temperature and may take up to 5 minutes for a cold unit. During warm-up, the unit blinks the two upper status lamps (44.1 and 48 light emitting diodes).

3. When set temperature is reached, the unit goes into self-calibration mode. The calibration time may take a few minutes. During calibration, the unit blinks the two lower status lamps (88.2 and 96 light emitting diodes).

4. The unit finds the first active input and converts digital audio to analog sound.

The DA924 figures out the incoming sample rate for the selected input and displays the incoming frequency (44.1, 48, 88.2 or 96KHz). When all inputs are inactive, the unit steps through the input ports continuously as indicated by the input select lamps if in auto select mode.

Most DACs contains relays for the purpose of muting the output during turn on (allowing the DAC to settle to proper operating conditions). The DA924 contains no relays, in order to avoid signal degradation associated with relay contacts. The unit deals with the turn on spike by incorporating very slow tracking power supplies for its output stage, thus disabling the drive capability during turn on. The DA924 turn on spike may be higher then that found in other DACs but the sound is not compromised. The spike due to power off is comparable to that found in other DACs.

Polarity inversion

The normal polarity is set to pin 2 hot. To invert, press the **POLARITY** switch. Signal inversion is indicated by a lit INVERT lamp.

Inverting while in unbalanced operation impacts signal polarity on the IEC center conductor.

Inverting while in unbalanced operation impacts signal polarity on pin 2 of the XLR connector.

Inverting while in balanced operation swaps pin 2 and pin 3 of the XLR connector.

CrystalLock™ and Wide lock

The DA924 **eliminates jitter** in the incoming data stream by use **CrystalLock™,** a DSP controlled pullable crystal oscillator and a short buffer memory for temporary storage of the incoming data. The DSP transfers the data from the memory to the DAC disregarding any jitter in the input frequency. A proprietary fast-lock high-accuracy measurement compares the average input frequency to the oscillator frequency and makes the appropriate adjustments. The

adjustments are done with sub pico-second resolution, to insure minimum interference with signal reconstruction.

CrystalLock™ meets and exceeds the AES lock range requirements (+/- 100ppm). Such narrow lock allows the use of pullable crystal oscillators, thus yielding the best performance from a jitter standpoint. The DA924 provides a wide lock mode for tracking sample rates between 40 and 50KHz, and 86 and 98kHz. Clock jitter levels increase when using varispeed, thus its use should be restricted for sample rates outside of the narrow lock range. Some multi-channel uses of the DA924 may require varispeed for synchronization.

To enable wide lock, press and hold the **POLARITY** button for 1.5 seconds. To return to **CrystalLock™**, press and hold the **POLARITY** button again. The unit indicates varispeed mode by blinking the appropriate status light periodically. This mode setting is retained when power is removed.

Part II: Theory of Operation

The simplified block diagram (figure 1) shows the basic building blocks.

Oven control

The PCM DAC is constructed of custom made laser trimmed thin film resistor networks; yet any resistor is subject to short term drift due to temperature variations and long term drift due to component aging. The resistor networks are kept at a constant temperature by a linearly controlled heating element. (A bang-bang controller, such as a home thermostat is undesirable because it produces turn on and turn off surges-- thus audible kicks.) Keeping the resistors at constant temperature overcomes resistor dependency on environmental temperature variations.

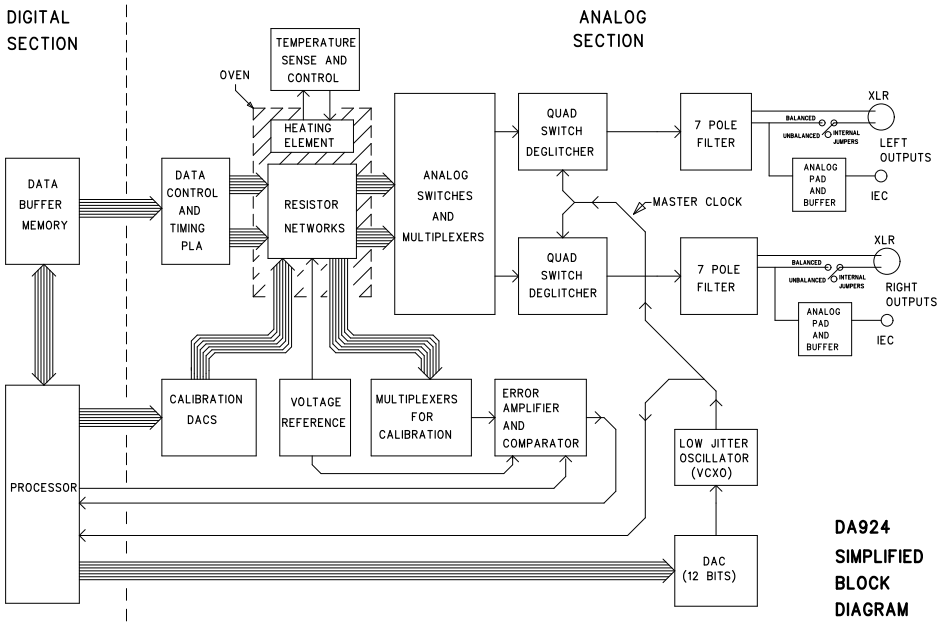

Figure 1

Calibration

A sequence where each resistor is tapped (one at a time) for voltage comparison against a reference level tells the processor the required adjustments. The voltage difference between any given network node and the reference is greatly amplified and then fed to a strobing comparator (see multiplexers for calibration and error amplifier and comparator gain blocks in the simplified diagram). The processor strobes the comparator and reads its output. The strobing is repeated 4000 times for the sake of averaging out any error due to amplifier noise. At the end of a comparator strobing cycle, the processor decides whether to increase or decrease the specific voltage of the measured node. This is done via the calibration 14 bit DACs (see diagram). Each calibration DAC is used as a 13 bit device to ensure monotonic performance. Each DAC is fed to its corresponding node through a large value resistor, thus a full 10V swing on the calibration DAC can only pull a given node by +/-4mV, providing an effective adjustment of a part in 5 million per calibration DAC step.

The calibration process takes a long time because the node adjustment is interactive (adjusting a node causes some misadjustment at all the other nodes). A single calibration cycle consists of reading and adjusting of all the nodes. The processor repeats the calibration cycle numerous times until all the nodes are set properly. Though nodes interaction exist during the adjustment process, the overall network is guaranteed to converge on a solution by design. Calibrating a DA924 for the first time (at the factory) often exceeds 25 minutes. Once calibrated, the settings are stored in non volatile ram for future startup point of reference, thus all future adjustments are initialized to the last settings. Therefore the initial tolerance of the components is pre calibrated already, and each new calibration needs to deal only with component drift under the same given temperature conditions (ovenized components). The remaining calibration at each subsequent power on takes less then 2 minutes typically.

Timing and deglitcher

The conversion from a digital sample value to an analog voltage consists of translating a digital code to a corresponding setting of analog switches and multiplexers to tap the appropriate voltage from the analog nodes. Such switching causes unwanted glitch energy to come into play. The glitch energy is code and signal dependent and can not be removed by filtering. The purpose of the deglitcher circuit (see diagram) is to block the signal from feeding to the output for long enough time after each transition, thus allowing the glitches enough time to disappear, and for each new analog sample to accurately settle to its final value.

The deglitcher circuit is in off state about half a sample time, and on for the rest of the time. The on time is the critical time and no digital activity takes place anywhere near the analog circuits. The settled signals are fed to the output filter with minimum disturbance. The deglitcher off time settling requires the circuit to block as much of the transitions from feeding forwards to the output filter.

The blocking requirement is very demanding because a transition of many volts between two adjacent sample values should feed forward less than a microvolt. A single switch can not yield such blocking performance. The deglitcher utilizes four switches: the first switch shunt (shorts) the signal to ground. The remaining signal is connected to the second switch that is in open state. Whatever comes through is shunted to ground be the third switch. The remaining tiny energy is further blocked by the fourth opened series switch.

During the deglitcher on state, the shunt switches (switch one and three) are opened and the series switches (switch two and four) are shorted to allow the signal path to the output. The deglither circuit utilizes DMOS technology thus providing extremely low resistance during the on state. The remaining problems due to on state resistance variations is neutralized by use of the strong feedback of the deglitcher amplifier.

The main reason for using DMOS transistors is their sub nanosecond switching capabilities. The jitter critical timing point is all at the deglitcher circuit. Each sample value must exist over the same time period thus precise deglitcher turn on and turn off are critical for good results. In fact switching during deglitcher blocking time can be somewhat sloppy, as long as the signals are well settled prior to turn on. Fighting the jitter wars means feeding the deglitcher circuit a precise jitter free on / off drive signal.

Jitter removal

Ordinary phase lock loops circuits (PLLs) do a reasonable job at removing high frequency jitter from the incoming clock. The same circuits perform very poorly in the removal of low frequency jitter from the clock signal. The need to keep enough bandwidth for locking to and tracking the incoming data translates to zero rejection of low frequency jitter content (typically hundreds of Hz of zero rejection bandwidth). While some of the jitter content is random, much is due to coupling of the data itself into the receiver circuitry.

The DA924 uses a non standard approach for removing jitter. The deglitcher circuit is clocked by a pullable crystal oscillator but the control signal for the crystal is freed from having to track down incoming clock variations. The clock oscillator is controlled by a processor driven DAC (not an ordinary phase detector plus filter circuit). The oscillator frequency is change by tiny amounts (.1ppm) and not very often (15 seconds or more) in a manner allowing it to track only very long term average drift. Using such an approach with ordinary PLL will cause loss of lock because the slight variations in incoming data rate cause loss of correspondence between the input and the too steady of a clock circuit. The DA924 CrystalLock (TM) approach, stores enough data in a dedicated memory to guarantee that each clock cycle can find its data. Moving the clock slowly to track the long-term average drift is done just fast enough to make sure that the buffer memory does not overfill or becomes empty.

At first glance, one may get concerned about the potential long delay due to storage of many data samples. In fact, the data storage is very small and so is the delay. An "unrealistic" 100ppm per second input rate step requires pre storage of about 5 words of data for 1 second D/A stepping, or an 50 word memory for 10 seconds of D/A update rate.

Output filter and drivers

The DA924 operates in low oversampling to allow for maximum settling time of the DAC circuits and to further reduce sensitivity to jitter. The upsampling filter is calculated by the DSP. The tradeoff in favor of low oversampling operation pauses an increased requirement for analog anti imaging filtering. The DA924 incorporates a seven pole analog filter.

The transistor based output drivers are short circuit protected and are capable of driving balanced 300 Ohm loads. As always, for best results it is recommended to use high quality cables. When running a cable through an electrically noisy environment, a termination impedance of 600 Ohms (at the destination, not at the DA924 side) may prove useful.

Power and Fusing

The Model DA924 operates at 50 or 60 Hz, and has two line voltage selections, 115 volts and 220 volts, switchable on the back panel. 115 volts operation requires a 1/2 ampere 250 volt fast blow fuse; 220 volt operation requires 1/4 ampere 250 volt fast blow fuse. Both American and European size fuses can be accommodated. Two fuses are required.

Operation up to 240 volts is possible with no change in performance using the 220 volt setting. Optimal operation requires 115 volts AC.

Maintenance

The Model DA924 is an auto-calibrating converter requiring no periodic adjustments. The unit's reliance on linear power supplies and discrete class A analog circuitry generates a significant amount of heat (25 watts maximum). The temperature rise is no cause for concern, but allowing for some airflow is always a benefit from a long-term reliability standpoint.

The front panel is gold plated (24 karat gold). Use a soft cloth (and plain water, if necessary) to clean fingerprints.

Part III: Specifications

Noise	-110dBFS rms, 130dBFS peak spurious response
Distortion	1kHz tone at -1dBFS: .0009% FS peak harmonic amplitude 1kHz tone at -60dBFS: .00009% FS peak harmonic amplitude 10kHz tone at -1dBFS: .0009% FS peak harmonic amplitude 10kHz tone at -60dBFS: .00009% FS peak harmonic amplitude
Sample rate	96kHx, 88.1kHz, 48kHz, 44.1kHz at +/- 150ppm lock range 40-50kHz wide lock mode (varispeed)
Crystal lock™ tracking	1ppm / 15 seconds
Channel separation	-100dBFs at 1KHz
Flatness response	+/- .05dB (10Hz -20KHz)
Phase linearity	2 degrees (10Hz - 20 KHz)
Digital inputs	Two AES/EBU, 110 Ohm, transformer isolated One Consumer, 75 Ohm, transformer isolated
Analog outputs	AES/EBU balanced 22dBuFS into 600 ohms Max 12dBuFS Min AES/EBU unbalanced 16dBuFS into 600 ohms Max, 6dBuFS Min Consumer outputs 8.5dBuFS into 10k ohms Max -2.5dBuFS Min
Warm-up and initial calibration	10 minutes maximum
Hardware	19 inch rack mount, 1U high
Power Requirements	115V 60Hz or 220V 50Hz, 20 Watts
Options	Removable interface for future I/O hardware interface